65C02 INSTRUCTIONS

Modes

Ip	Implied	
Ac	Accumulator	
Im	Immediate	#$12
Z	ZeroPage	$12
Zx	ZeroPage,X	$12,X
Zy	ZeroPage,Y	$12,Y
Ab	Absolute	$1234
Ax	Absolute,X	$1234,X
Ay	Absolute,Y	$1234,Y
R	Relative	LABEL
Ix	Ind, zp X	($12,X)
IAx	Ind, abs X	($1234,X)
Iy	Ind, zp Y	($12),Y
Iz	Ind, zp	($12)
Ia	Ind, abs	($1234)

Load & Store

LDA NVBDIZC
LoaD Accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

LDX NVBDIZC
LoaD X register
Im^{2} Z^{3} Zy^{4} Ab^{4} Ay^{4+}

LDY NVBDIZC
LoaD Y register
Im^{2} Z^{3} Zx^{4} Ab^{4} Ay^{4+}

STA NVBDIZC
STore Accumulator
Z^{3} Zx^{4} Ab^{4} Ax^{5+} Ay^{5+} Ix^{6} Iy^{6} Iz^{5}

STX NVBDIZC
STore X register
Z^{3} Zy^{4} Ab^{4}

STY NVBDIZC
STore Y register
Z^{3} Zx^{4} Ab^{4}

STZ NVBDIZC
STore Zero
Z^{3} Zx^{4} Ab^{4} Ax^{5+}

State

CLC NVBDIZC
CLear Carry
Ip^{2}

CLD NVBDIZC
CLear Decimal
Ip^{2}

CLI NVBDIZC
CLear Interrupt
Ip^{2}

CLV NVBDIZC
CLear oVerflow
Ip^{2}

SEC NVBDIZC
SEt Carry
Ip^{2}

SED NVBDIZC
SEt Decimal
Ip^{2}

SEI NVBDIZC
SEt Interrupt
Ip^{2}

Bits

ASL NVBDIZC
Arithmetic Shift Left
Ac^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7+}

LSR NVBDIZC
Logical Shift Right
Ac^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7+}

ROL NVBDIZC
ROtate Left
Ac^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7+}

ROR NVBDIZC
ROtate Right
Ac^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7+}

AND NVBDIZC
bitwise AND with accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

ORA NVBDIZC
bitwize OR with Accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

EOR NVBDIZC
bitwise Exclusive OR
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

BIT NVBDIZC
test BITs
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+}

CMP NVBDIZC
CoMPare accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

CPX NVBDIZC
ComPare X register
Im^{2} Z^{3} Ab^{4}

CPY NVBDIZC
ComPare Y register
Im^{2} Z^{3} Ab^{4}

TRB NVBDIZC
Test and Reset Bits
Z^{5} Ab^{6}

TSB NVBDIZC
Test and Set Bits
Z^{5} Ab^{6}

RMB NVBDIZC
Reset Memory Bit
Z^{5} Ab^{6}

SMB NVBDIZC
Set Memory Bit
Z^{5} Ab^{6}

Flow

JMP NVBDIZC
JuMP
Ab^{3} Ia^{5+} IAx^{6+}

JSR NVBDIZC
Jump to SubRoutine
Ab^{6}

RTS NVBDIZC
ReTurn from Subroutine
Ip^{6}

RTI NVBDIZC
ReTurn from Interrupt
Ip^{6}

BRA NVBDIZC
BRanch Always
R^{3}

BEQ NVBDIZC
Branch on EQual
R^{2}

BNE NVBDIZC
Branch on Not Equal
R^{2}

BCC NVBDIZC
Branch on Carry Clear
R^{2}

BCS NVBDIZC
Branch on Carry Set
R^{2}

BVC NVBDIZC
Branch on oVerflow Clear
R^{2}

BVS NVBDIZC
Branch on oVerflow Set
R^{2}

BMI NVBDIZC
Branch on MInus
R^{2}

BPL NVBDIZC
Branch on PLus
R^{2}

BBR<0-7> NVBDIZC
Branch on Bit Reset
R^{2}

BBS<0-7> NVBDIZC
Branch on Bit Set
R^{2}

Stack

PHA NVBDIZC
PusH Accumulator
Ip^{3}

PHX NVBDIZC
PusH X register
Ip^{3}

PHY NVBDIZC
PusH Y register
Ip^{3}

PHP NVBDIZC
PusH Processor status
Ip^{3}

PLA NVBDIZC
PuLl Accumulator
Ip^{4}

PLP NVBDIZC
PuLl Processor status
Ip^{4}

PLX NVBDIZC
PuLl X register
Ip^{4}

PLY NVBDIZC
PuLl Y register
Ip^{4}

TXS NVBDIZC
Transfer X to Stack
Ip^{2}

TSX NVBDIZC
Transfer Stack to X
Ip^{2}

Transfer

TAX NVBDIZC
Transfer A to X
Ip^{2}

TAY NVBDIZC
Transfer A to Y
Ip^{2}

TXA NVBDIZC
Transfer X to A
Ip^{2}

TYA NVBDIZC
Transfer Y to A
Ip^{2}

Calc

INA NVBDIZC
INcrement Accumulator
Ac^{2}

INX NVBDIZC
INcrement X
Ip^{2}

INY NVBDIZC
INcrement Y
Ip^{2}

DEA NVBDIZC
DEcrement Accumulator
Ac^{2}

DEX NVBDIZC
DEcrement X
Ip^{2}

DEY NVBDIZC
DEcrement Y
Ip^{2}

INC NVBDIZC
INCrement memory
Z^{5} Zx^{6} Ab^{6} Ax^{7+}

DEC NVBDIZC
DECrement memory
Z^{5} Zx^{6} Ab^{6} Ax^{7+}

ADC NVBDIZC
ADD with Carry
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

SBC NVBDIZC
SuBtract with Carry
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5} Iz^{5}

Misc

BRK NVBDIZC
BReaK
Ip^{7}

NOP NVBDIZC
No OPeration
Ip^{2}

STP NVBDIZC
SToP
Ip^{3}

WAI NVBDIZC
WAit for Interrupt
Ip^{3}

Flags (Right Upper corner): N=Negative, V=Overflow, B=Break, D=Decimal, I=Interrupt Disable, Z=Zero, C=Carry. Green flags are affected by the instruction.

Timing: The green number next to each mode is the number of CPU cycles for that addressing mode. A "+" means an extra cycle may be used (e.g. on page crossing).