6502 INSTRUCTIONS

Modes

Ip	Implied	
Ac	Accumulator	
Lb	Label	LABEL
Im	Immediate	#$12
Z	Zero Page	$12
Zx	Zero Page,X	$12,X
Zy	Zero Page,Y	$12,Y
Ab	Absolute	$1234
Ax	Absolute,X	$1234,X
Ay	Absolute,Y	$1234,Y
In	Indirect	($1234)
Ix	Indirect,X	($12,X)
Iy	Indirect,Y	($12),Y

ADC NVBDIZC
ADD with Carry
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

AND NVBDIZC
bitwise AND with accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

ASL NVBDIZC
Arithmetic Shift Left
A^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7}

BIT NVBDIZC
test BITs
Z^{3} Ab^{4}

BPL NVBDIZC
Branch on PLus
Lb^{2+}

BMI NVBDIZC
Branch on MInus
Lb^{2+}

BVC NVBDIZC
Branch on oVerflow Clear
Lb^{2+}

BVS NVBDIZC
Branch on oVerflow Set
Lb^{2+}

BCC NVBDIZC
Branch on Carry Clear
Lb^{2+}

BCS NVBDIZC
Branch on Carry Set
Lb^{2+}

BNE NVBDIZC
Branch on Not Equal
Lb^{2+}

BEQ NVBDIZC
Branch on EQual
Lb^{2+}

BRK NVBDIZC
BReaK
Ip^{7}

CMP NVBDIZC
CoMPare accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

CPX NVBDIZC
ComPare X register
Im^{2} Z^{3} Ab^{4}

CPY NVBDIZC
ComPare Y register
Im^{2} Z^{3} Ab^{4}

DEC NVBDIZC
DECrement memory
Z^{5} Zx^{6} Ab^{6} Ax^{7}

EOR NVBDIZC
bitwise Exclusive OR
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

CLC NVBDIZC
CLear Carry
Ip^{2}

SEC NVBDIZC
SEt Carry
Ip^{2}

CLI NVBDIZC
CLear Interrupt
Ip^{2}

SEI NVBDIZC
SEt Interrupt
Ip^{2}

CLV NVBDIZC
CLear oVerflow
Ip^{2}

CLD NVBDIZC
CLear Decimal
Ip^{2}

SED NVBDIZC
SEt Decimal
Ip^{2}

JMP NVBDIZC
JuMP
Ab^{3} In^{5}

JSR NVBDIZC
Jump to SubRoutine
Ab^{6}

LDA NVBDIZC
LoaD Accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

LDX NVBDIZC
LoaD X register
Im^{2} Z^{3} Zy^{4} Ab^{4} Ay^{4+}

LDY NVBDIZC
LoaD Y register
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+}

LSR NVBDIZC
Logical Shift Right
A^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7}

NOP NVBDIZC
No OPeration
Ip^{2}

ORA NVBDIZC
bitwize OR with Accumulator
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

TAX NVBDIZC
Transfer A to X
Ip^{2}

TXA NVBDIZC
Transfer X to A
Ip^{2}

DEX NVBDIZC
DEcrement X
Ip^{2}

INX NVBDIZC
INcrement X
Ip^{2}

ROL NVBDIZC
ROtate Left
A^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7}

ROR NVBDIZC
ROtate Right
A^{2} Z^{5} Zx^{6} Ab^{6} Ax^{7}

RTI NVBDIZC
ReTurn from Interrupt
Ip^{6}

RTS NVBDIZC
ReTurn from Subroutine
Ip^{6}

SBC NVBDIZC
SuBtract with Carry
Im^{2} Z^{3} Zx^{4} Ab^{4} Ax^{4+} Ay^{4+} Ix^{6} Iy^{5+}

STA NVBDIZC
STore Accumulator
Z^{3} Zx^{4} Ab^{4} Ax^{5} Ay^{5} Ix^{6} Iy^{6}

TXS NVBDIZC
Transfer X to Stack
Ip^{2}

INC NVBDIZC
INCrement memory
Z^{5} Zx^{6} Ab^{6} Ax^{7}

TAY NVBDIZC
Transfer A to Y
Ip^{2}

TYA NVBDIZC
Transfer Y to A
Ip^{2}

DEY NVBDIZC
DEcrement Y
Ip^{2}

INY NVBDIZC
INcrement Y
Ip^{2}

TSX NVBDIZC
Transfer Stack to X
Ip^{2}

PHA NVBDIZC
PusH Accumulator
Ip^{3}

PLA NVBDIZC
PuLl Accumulator
Ip^{4}

PHP NVBDIZC
PusH Processor status
Ip^{3}

PLP NVBDIZC
PuLl Processor status
Ip^{4}

STX NVBDIZC
STore X register
Z^{3} Zy^{4} Ab^{4}

STY NVBDIZC
STore Y register
Z^{3} Zx^{4} Ab^{4}

Flags (Right Upper corner): N=Negative, V=Overflow, B=Break, D=Decimal, I=Interrupt Disable, Z=Zero, C=Carry. Green flags are affected by the instruction.

Timing: The green number next to each mode is the number of CPU cycles for that addressing mode. A "+" means an extra cycle may be used (e.g. on page crossing).